Non-retention of Cache RAM Data During Deep Sleep

1. Introduction

This document describes a silicon issue discovered in a single returned device with a cache RAM array that does not retain all of its values during deep sleep mode.

2. Affected Devices

This issue was seen on only one part, but it is possible that it may occur on any version or package of Apollo3 Blue MCU silicon, AMA3B1KK-xxx, up to and including silicon revision B0.

3. Issue Details

It was seen in this cache RAM array data retention issue that data was correct in the cache before entry into deep sleep mode, but was invalid immediately after exiting deep sleep upon interrupt. If normal sleep is entered, or the voltage is forced during deep sleep to be normal operating voltage, then data is retained. Only one of the nine cache RAM banks showed this issue so it does not appear to be a control or voltage issue when putting the banks of RAM into deep sleep. The failing RAM was consistently having the same bit flip to 1 during deep sleep, so it appears to be a silicon issue with this particular chip.

4. Application Impact

The application impact of this issue of not retaining data in cache RAM through deep sleep transitions is causing the CPU to execute incorrect instruction data instead of the correct data stored in internal Flash. This is manifested in the occurrence of INVSTATE and NOCP faults.

5. Workarounds

Since this issue has occurred on a single device due to a single errant bit in a cache RAM array, the conclusion is that this is not a systematic issue, and therefore a generally applied workaround is not warranted. However, if it is required or desired to reduce the likelihood of this issue occurring on other devices, the following precaution could be applied.

To assure retention of data in cache RAM through deep sleep transitions, disable the cache during deep sleep by setting the CACHEPWDSLP bit in the Power Control module's MEMPWRDINSLEEP register. When this is done, the cache essentially gets powered down during deep sleep mode, then auto-initializes again after waking. This process takes very little additional power reloading the cache, and is likely offset by the power saving of the cache being powered down during deep sleep.

6. Resolution Status

There are no plans to address this issue in a silicon revision, as this is believed to be an isolated incident involving a single bit-flip anomaly in a single device. The referenced precaution in the above Workaround section adequately prevents the issue from occurring.

Classification: Test escape

7. Document Revision History

Rev #	Description
1.0	Initial version

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